Amendments to the Specification

Please amend ¶ [0025] on page 7 of the (substitute) specification as follows:

[0025] In a program sequence, before outputting from the sequence memory 9, the program word 17 having a set bit 21 contained therein is checked for an active state. If such a state is identified, the further program word processing in the instruction word generation processor 10 is interrupted and the information part of this program word 17 is written to a read pointer register 18, a write pointer register 19 and a block length register 20.

Please amend ¶ [0027] on pages 7-8 of the (substitute) specification as follows:

[0027] During the subsequent instruction word processing in an instruction word memory 24 preferably having first and second instruction word memory page 6, 7, one of which is selected by the content of the page register 27, the output read pointer 35 specifies the current reading row number and the output write pointer 36 specifies the current writing row number of a block of instruction words which is to be processed, and which is provided with the block length determined by the content of the block length register 20. The instruction word processing step can be executed in accordance with the program by means of read/write/NOP (no-operation) operations, connected with a required outputting operation into the instruction word output 11.

Please amend ¶ [0031] on pages 8-9 of the (substitute) specification as follows:

[0031] If, during an instruction word processing, no new instruction word 15 is requested by the instruction word generation <u>processor</u> 10 for storage in the instruction word memory 24, the program word successor 16 from the sequence memory 9 and the instruction word 15 currently output by the instruction word memory 24 are read in by the prefetch unit 28 and the additional instruction word 29 is generated.

Please amend ¶ [0032] on page 9 of the (substitute) specification as follows:

[0032] The latter is provided in a free row of the instruction word memory 24 or in the additional instruction word memory 30, and is immediately reloaded in the event of a request for a new instruction word 15 that is effected in the further course of the instruction word processing. The delay during the provision of the new instruction word 15 in the instruction word generation <u>processor</u> 10, caused by the processing time arising there, is avoided in this way.

Please amend ¶ [0033] on page 9 of the (substitute) specification as follows:

[0033] The functions required for processing in the corresponding functional units ~~10~~ <u>12</u> of the processor 13 are triggered with storage of the instruction word 15 in the instruction word output 11.